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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,374	02/02/2000	Masami Kidono	OOCL-11 (11P024627)	6123

26479 7590 11/16/2005

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EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/496,374	KIDONO ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 8 September 2003. These drawings are acceptable.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Recently amended independent claims 1-6 each newly recite the limitation, "and N also being the minimum periodic unit of connections from said gate electrodes to said connection terminals within said successive pixel rows." However, the examiner respectfully notes such subject matter was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. For instance, Figure 3 of the

instant invention illustrates N=16 gate electrode groups (see also page 20 of the amendment filed 15 April 2002). Figure 3 clearly illustrates gate electrodes 15a and 13a being commonly connected to connection terminal 13. As such, the connection from gate electrode 13a to connection terminal 13 is seen as repeating itself at gate electrode 15a. In such a manner, N=16 cannot be said to constitute the minimum period of this repeating pattern.

5. Claims 7-9 and 12-25 are rejected under 35 U.S.C. 112, first paragraph, as being dependent upon rejected base claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1-9 and 12-25 are rejected under 35 U.S.C. 102(a) as being anticipated by Yanai et al (JP 10-150601 A -- and as recited as the current application's own admitted prior art -- see Page 5, Line 14 of the instant application). Note: For clarity of comparison's sake, the following rejection refers to the reference numerals and figures as illustrated in the background of the instant invention. However, for completeness, a separate English translation of Yanai has been included with this Office Action.

Regarding claim 1, Yanai (as recited in the background of the current invention) discloses a solid-state imaging device comprising: a pixel unit [Fig. 7, 1] constituted by a two-

dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time; a vertical transfer unit [Fig. 7, 2] for vertically transferring charge from the pixels in the pixel unit; a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit; shift gates [Fig. 7, 3] each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes [Fig. 7, 4A -- horizontal lines] for controlling the shift gates; and a plurality of lead lines [Fig. 7, 4A -- vertical lines] for connecting the gate electrodes to an external circuit and a plurality of connection terminals [Fig. 7, 6] for connecting the gate electrodes to the external circuit; the gate electrodes making up N [where N = 6, for instance] of gate electrode groups in which the lines belonging to each coset of modulo 6 within successive pixel rows are connected to common lead lines, 6 being a predetermined natural number between 4 and one half the number of pixels [where the number of pixels = 12, for instance] in a column, and N also being the minimum periodic unit of connections from the gate electrodes to the connection terminals within the successive pixel rows, the gate electrodes having common connection terminals to reduce the number (i.e. from 3 to 2, for instance) of the connection terminals to less than 12, and enable the gate electrodes having common connection terminals to be controlled with different timing of non-common connection terminals of the gate electrode groups (see Page 2, Line 15 - Page 5, Line 6 of the instant invention, as well as the full disclosure of Yanai).

Regarding claim 2, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, Yanai (as recited in the background of the current invention)

discloses gate electrodes/gate control lines [Fig. 7, 4A] connected to gate electrode groups in which horizontal lines belonging to each coset of modulo 6 [where N=6, for instance] within successive pixel rows are connected commonly, being combined with each other so as to reduce the number (i.e. from 3 to 2, for instance) of the connection terminals to less than 6 (see Page 2, Line 15 - Page 5, Line 6 of the instant invention, as well as the full disclosure of Yanai).

Regarding claim 3, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, Yanai (as recited in the background of the current invention) discloses the gate electrodes being provided in a predetermined number 6 [where N = 6, for instance] of gate electrode groups such that the horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo 6, 6 being a predetermined natural number between 4 and one half the number of pixels [where the number of pixels = 12, for instance] in a column, and N also being the minimum periodic unit of connections from the gate electrodes to the connection terminals within the successive pixel rows, some of the gate electrode groups being commonly connected so that the connection electrodes are less in number (i.e. from 3 to 2, for instance) than 6, and enable the gate electrodes having common connection terminals to be controlled with different timing of non-common connection terminals of the gate electrode groups (see Page 2, Line 15 - Page 5, Line 6 of the instant invention, as well as the full disclosure of Yanai).

Regarding claim 4, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, Yanai (as recited in the background of the current invention)

discloses the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving (see Fig. 7; Page 4, Line 8 - Page 5, Line 6 of the instant invention, as well as the full disclosure of Yanai).

Regarding claim 5, this claim is rejected under the reasoning applied in the above rejection of claims 1, 2 and 4.

Regarding claim 6, this claim is rejected under the reasoning applied in the above rejection of claims 1, 3 and 4.

Regarding claims 7-9, Yanai (as recited in the background of the current invention) discloses gate electrode groups controlled in each of all the predetermined read-out modes are set such as to provide a minimum number of connection terminals for connecting the gate electrodes to an external circuit (see Fig. 7; Page 4, Line 8 - Page 5, Line 6 of the instant invention, as well as the full disclosure of Yanai; where 2 connection terminals is the minimum in this modulo 6 example).

Regarding claims 12-17, Yanai (as recited in the background of the current invention) discloses at least two horizontal lines belonging to the same pixel group but to different gate electrode groups are connected to a common connection terminal (see Fig. 7; Page 2, Line 15 - Page 5, Line 6 of the instant invention, as well as the full disclosure of Yanai).

Regarding claims 18-23, Yanai (as recited in the background of the current invention) discloses only two connection terminals connected to the vertical transfer unit are not connected to any of the gate electrodes (see Fig. 7; Page 2, Line 15 - Page 5, Line 6 of the instant invention, as well as the full disclosure of Yanai).

Regarding claim 24, Yanai (as recited in the background of the current invention) discloses connections from the gate electrodes to the connection terminals within successive pixel rows have a periodic repetition, and wherein N is the minimum period of repetition (see Fig. 7; Page 2, Line 15 - Page 5, Line 6 of the instant invention, as well as the full disclosure of Yanai).

Regarding claim 25, Yanai (as recited in the background of the current invention) discloses connections from the gate electrodes to the connection terminals within successive pixel rows exhibit a repeating pattern, and wherein N is the minimum period of the repeating pattern (see Fig. 7; Page 2, Line 15 - Page 5, Line 6 of the instant invention, as well as the full disclosure of Yanai).

Response to Arguments

8. Applicants' arguments filed 21 October 2005 have been fully considered but they are not persuasive. The applicants argue the claimed invention -- particularly in regards to the subject matter of N *"being the minimum periodic unit of connections from said gate electrodes to said*

connection terminals within said successive pixel rows" -- is fully supported by the instant specification. However, the examiner respectfully disagrees. The applicants dispute the examiner's position that the minimum periodic unit of connections from said gate electrodes [Fig. 7, 4A -- horizontal lines] to said connection terminals [Fig. 7, 6] within said successive pixel rows [Fig. 7, 1] is 2, because *"the connection is not repeated every 2 gate electrodes"* (see Page 13 of the applicants' arguments submitted 21 October 2005). The examiner appreciates the applicants' point, and agrees *"the connection is not repeated every 2 gate electrodes."* However, gate electrode #13a and gate electrode #15a are commonly connected to connection terminal #13. And this shared circuitry arrangement is indeed repeated at a regular interval/period (every sixteen pixels). Furthermore, in the context of the claim language in question, the length of this interval/period is a moot point. It only matters that there exists *some/any* degree of periodicity.

The applicants also contend Yanai (as recited in the background of the current invention) does not teach that N is the minimum periodic unit of connections from said gate electrodes to said connection terminals within said successive pixel rows (see Fig. 7; page 14 of applicants' arguments submitted 21 October 2005; and the drawing attached to the applicants' arguments submitted 3 November 2004). However, the examiner respectfully disagrees. In the discussed example (again, see page 13 of applicants' arguments submitted 3 November 2004) where N = 272 gate electrode groups, it would simply not be possible to connect all 272 gate electrodes [Fig. 7, 4A -- horizontal lines] to the connection terminals [Fig. 7, 6] with any fewer than 272 connections.

Lastly, the applicants contend Yanai (as recited in the background of the current invention) neglects enabling the gate electrodes having common connection terminals to be

controlled with different timing of non-common connection terminals of the gate electrode groups. However, the examiner respectfully disagrees. Yanai's "independent gate pulse application lead lines" [Fig. 7; 4A], by way of being *independent* from non-common connection terminals inherently enable the gate electrodes having common connection terminals to be controlled with different timing of non-common connection terminals of the gate electrode groups (see Page 5, Lines 1-6 of the instant invention).

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yanai (US 6,760,069 B2), Kondo et al (US 6,476,941 B1), and Udagawa et al (US 5,880,781 A) are cited to further evidence the state of the art pertaining to solid-state imaging devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J.P.
8 November 2005

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